DAILYASSESSMENTFORMAT

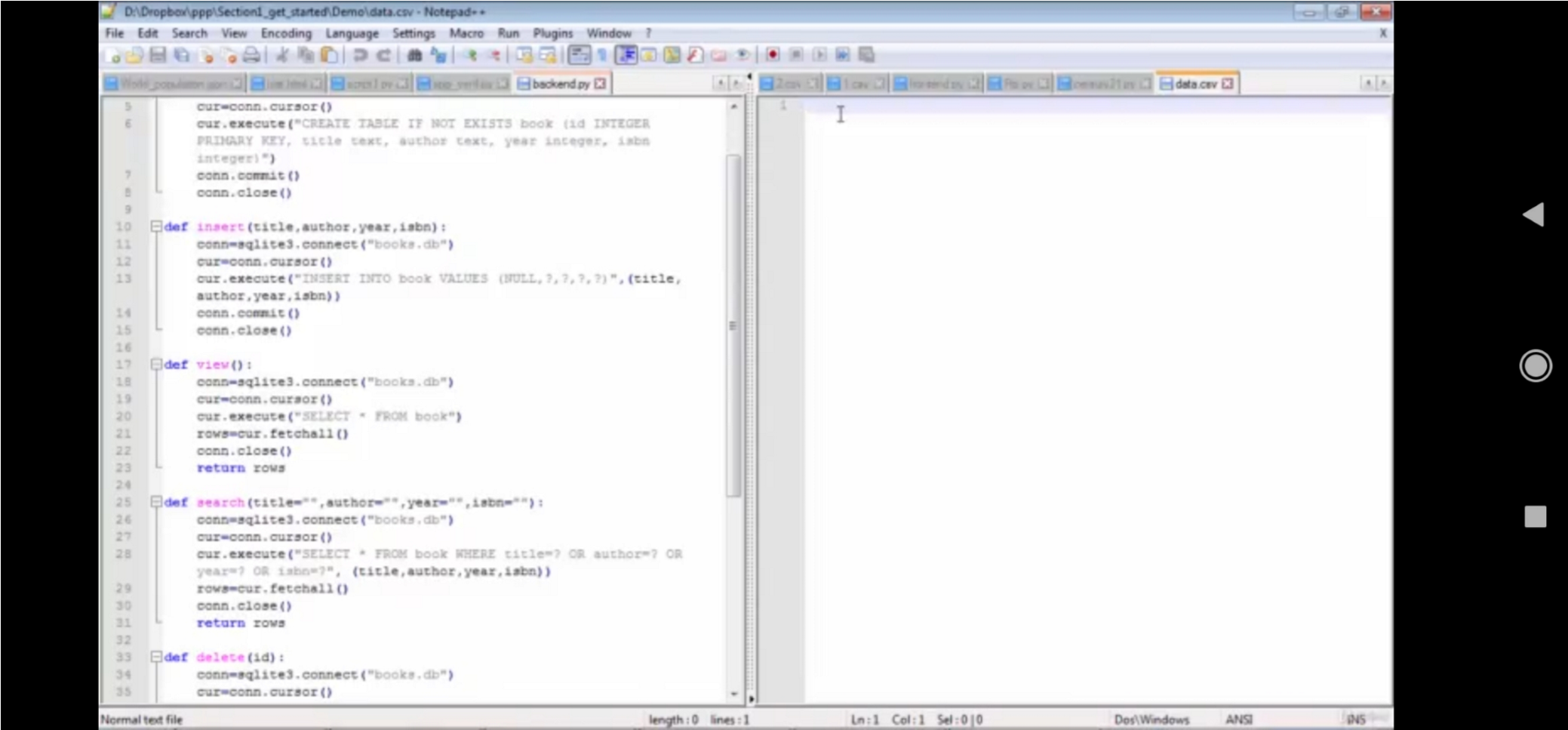
|  |  |  |  |
| --- | --- | --- | --- |
| Date: | 02-06-2020 | Name: | Rachana C Hulikatti |
| Course: | DIGITALDESIGNUSINGHDL | USN: | 4AL17EC108 |
| Topic: | FPGABasics:Architecture, ApplicationsandUses  VerilogHDLBasicsbyIntel VerilogTestbenchcodeto  verifythedesignundertest  (DUT) | Semester &Section: | 6thA-sec |
|  |  |  |  |
| FORENOONSESSIONDETAILS | | | |
| Imageofsession | | | |

|  |
| --- |
| Report–Reportcanbetypedorhandwrittenforuptotwopages.  FPGABasics:Architecture,ApplicationsandUsesVerilogHDL BasicsbyintelVerilogTestbenchcodetoverifythedesignunder test(DUT).  SpecificapplicationofanFPGAincludesdigitalsignalprocessing, bioinformatics,devicecontrollers,software-definedradio,random logic,ASICprototyping,medicalimaging,computerhardware emulation,integratingmultipleSPLDs,voicerecognition, cryptography,filteringandcommunicatione  Ncodingandmany  modulemux\_4to1\_case(input[3:0]a, //4-bitinput  calledainput[3:0]b, input[3:0]c, input[3:0]d, input[1:0]sel, betweena,b,c,doutputreg[3:0]out); always@(aorborcordorsel)begin case(sel)  2'b00:out<=a; 2'b01:out<=b;  2'b10:out<=c;  2'b11:out<=d; |
| FPGAsareparticularlyusefulforprototypingapplication-specific integratedcircuits(ASICs)orprocessors.AnFPGAcanbe reprogrammeduntiltheASICorprocessordesignisfinalandbugfreeandtheactualmanufacturingofthefinalASICbegins.Intel itselfusesFPGAstoprototypenewchips.  TheFPGAisFieldProgrammableGateArray.Itisatypeofdevice thatiswidelyusedinelectroniccircuits.FPGAsaresemiconductor deviceswhichcontainprogrammablelogicblocksand  interconnectioncircuits.Itcanbeprogrammedorreprogrammedto therequiredfunctionalityaftermanufacturing.  TheDeviceUnderTest(D.U.T.)Inthisexample,theDUTis behavioralVerilogcodefora4-bitcounterfoundinAppendixA.This isalsoknownasaRegisterTransferLevelorRTLdescriptionofthe design.IntheHDLsource,alltheinputandoutputsignalsare declaredintheportlist |

|  |
| --- |
| modulemux\_4to1\_case(input[3:0]a, //4-bitinput  calledainput[3:0]b, input[3:0]c, input[3:0]d, input[1:0]sel, betweena,b,c,doutputreg[3:0]out); always@(aorborcordorsel)begin case(sel)  2'b00:out<=a; 2'b01:out<=b;  2'b10:out<=c;  2'b11:out<=d; |

endcase end endmodule

|  |  |  |
| --- | --- | --- |
| Date: | 02-06-2020 Name: | JagadeeshaHegde |
| Course: | ThePythonMega USN:  Course | 4AL17EC036 |
| Topic: | InteractiveData Semester&  VisualizationwithBokeh Section:  Webscrapingwith Python  BeautifulSoup | 6thA-sec |
| AFTERNOONSESSIONDETAILS | | | | |
| Imageofsession | | | | |



|  |
| --- |
| Report–Reportcanbetypedorhandwrittenforuptotwopages.  SCRAPINGWITHPYTHONBEAUTIFULSOUP  Theincredibleamountofdataontheinternetisarichresourceofanyfieldidresearchor personalinternet.  Toeffectivelyharvestthedata,youllneedtobecomeskilledatwebscraping.  Thepythonlibrariesrequestsandbeautifulsoularepowerfultoolsforjob.ifyouliketo learnwithhandsonexamplesandyouhaveabasicunderstandingofpythonandHTML.  INTERACRIVEDATAVISUALIZATIONWITHBOKEH  Bokehpridesitselfonbeingalibraryforinteractivedatavisualization.  Unlikepopularcounterpartsinthepythonvisualizationspace,likematplotlibandseaborn, bokehrendersitsgraphicsusingHTMLandjavascripts. |